Code No: C7502 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I - Semester Examinations, April/May-2012
DIGITAL CONTROL SYSTEMS
(CONTROL SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1.a) With help of suitable circuit explain the principle of operation of sample and hold devices. Derive the transfer function of zero order hold circuit.

b) With suitable diagram explain any method of analog to digital conversion.

2.a) Find the z-transform of the following function x(k)

$x(k) = \sum_{h=0}^{k} a^k$, where '**a**' is a constant.

b) Find the inverse z-transform of the following functions:

(i) $X(z) = \frac{z^{-1}(1-z^{-2})}{(1+z^{-2})^2}$ and (ii) $X(z) = \frac{z-0.4}{z^2+z+2}$

3. The block diagram of a digital control system is shown in Figure 1, where $G_p(s) = \frac{K(s+5)}{s^2}$.

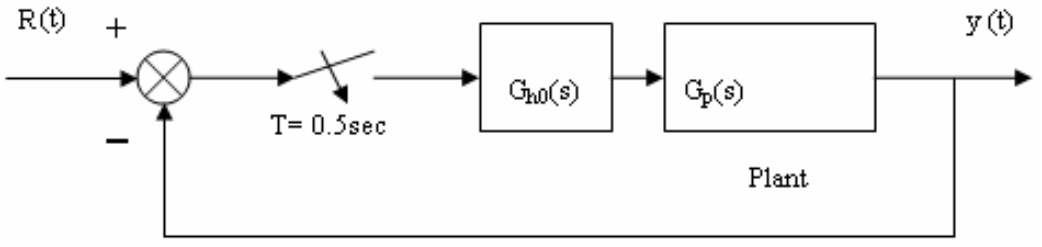

Figure 1

Determine the range of K for the system to be asymptotically stable.

4. For positive values of the gain, sketch the root locus for unity feedback sampled data system having the open loop transfer function:

$G(z) = \frac{K(z+0.1)^2}{(z-1)(z-0.9)(z-0.1)}$

For what value of the gain does the system become unstable?

Contd.....2

5. The block diagram of a discrete-data control system is shown in Figure 2, in which $G_p(s) = \dfrac{2}{s^2 + s + 2}$ and T = 1.0 sec. Compute and plot the unit step response $c^*(t)$ of the system. Find the step, ramp, and parabolic error constants. Also final value of c(kT).

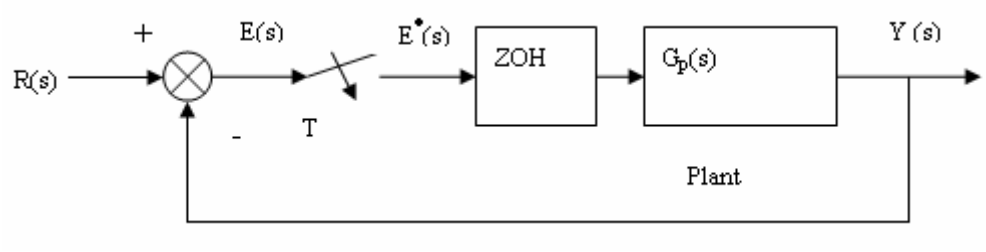

Figure 2

6. A block diagram of a digital control system is shown in Figure 3. Design a PID controller, D(z) to meet the following specifications: (i) Velocity error constant, $K_v \geq 10$, (ii) Phase margin $\geq 60^0$ and (iii) bandwidth = 8 rad./sec.

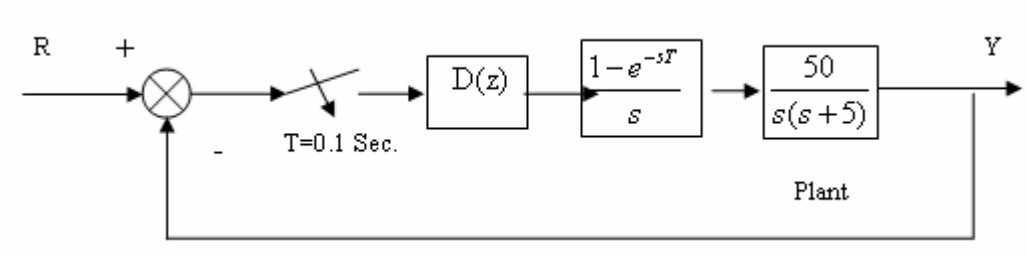

Figure 3

7. Find the state space representation of the following system:
$y(k + 2) – 3y(k + 1) + 2y(k) = 4^k$ and $y(0) = 0$; $y(1) = 1$.
Find the complete solution of the above system.

8.a) Derive the necessary condition for digital control system
$X(k+1) = G\,X(k) = Hu(k)$
$Y(k)=C\,X(k)$ to be output controllable and observable.

b) A digital process is described by the state equation

$$X(k + 1) = \begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix} X(k) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} U(k)$$

$y(k) = [2 \quad 0]X(k)$
Design the first-order observer so as to have a dead beat response.

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